Efficient Task Fusion Exploration for Data Intensive Computing SoC

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Abstract Design of data-intensive computing systems, such as radar/sonar and image processing systems, is a very challenging problem due to increasing of application complexity and system performance requirements. A crucial issue is the optimization of the communications and storage sub-system. Indeed, such a sub-system determines the overall achievable data parallelism and hardware efficiency. In this poster, we present a method using loop fusions to rapidly and effectively explore possible application mapping onto a configurable hardware architecture. The functionality of the application is given through an array-oriented representation and the configurable hardware architecture integrates pipelined-based processing elements, which communicate through FIFO queues and double buffering mechanisms. As a consequence, they are capable of performing parallel computations and data accesses, and they mask the latency of data accesses with the latency computations. A method based on integer partitions is used to reduce the complexity of fusion exploration (cf. figure 1). Thanks to this method, the number of comparisons needed to smartly explore all the possible fusions is extremely reduced; for the example of figure 1, it is reduced of 77%. Our proposition is illustrated on a case study implementing a hydrophone monitoring application (cf. figure 2).

Key words: Data-intensive computing, task fusion, hardware architecture design, design space exploration

References

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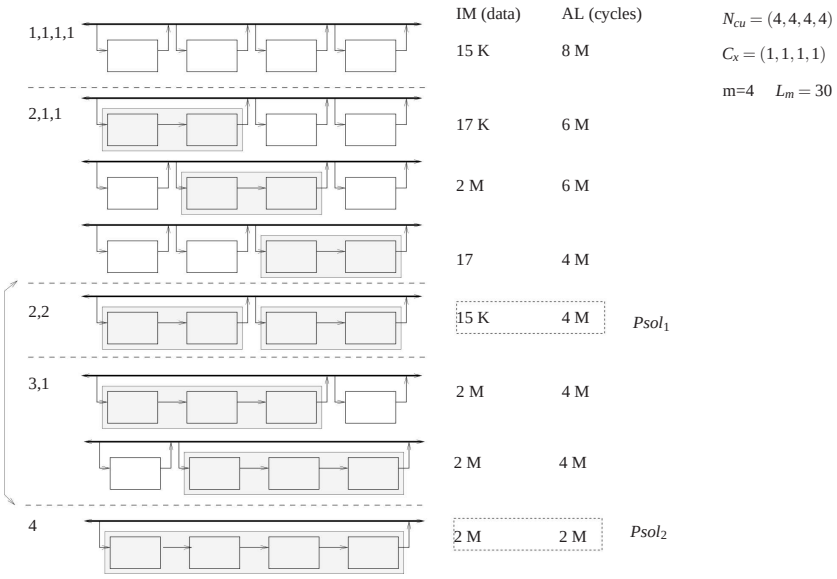

Fig. 1: Example of an exploration for a 4-tasks application. Dependencies impose to the solutions merging the 2 central tasks to use the largest internal memories.

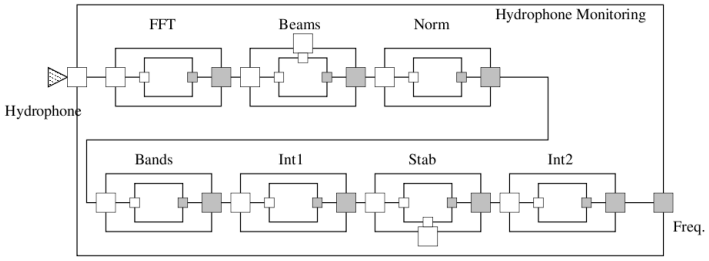

Fig. 2: Array-OL specification of a hydrophone monitoring application.

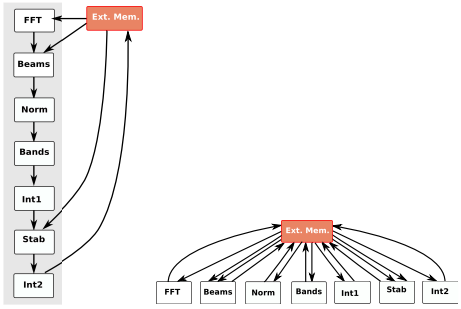

Fig. 3: Example of fusion configurations for the hydrophone monitoring application.