Automatic Architecture Synthesis and Application Mapping for Application-specific Customizable MPSoCs

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Abstract. The recent progress in modern nano-electronic technology enabled implementation of very complex multiprocessor systems on single chips and created a big push towards development of various kinds of high-performance embedded systems. However, the opportunities created can be effectively exploited only through use of more adequate system architectures and more integrated system IP modules, supported by new effective and efficient design methods and electronic design automation tools. This paper focuses on mastering the automatic development of heterogeneous MPSoCs based on customizable ASIPs and is related to the European project ASAM (Automatic Architecture Synthesis and Application Mapping).

Keywords: embedded systems, MPSoCs, customizable ASIPs, macro-/micro-architecture, architecture synthesis, application mapping, quality-driven design, model-based design, design space exploration, trade-off exploitation.

1 Introduction

The recent spectacular progress in modern nano-electronic technology enabled implementation of very complex multiprocessor systems on single chips and created a big push towards development of various kinds of high-performance embedded systems. Increasingly complex and sophisticated embedded systems are required to perform real-time computations to extremely tight schedules with high demands regarding energy, power, area, and cost efficiency. Additionally, these systems are required to be flexible enough to enable adequate reuse among different product versions, reaction to market shifts, adherence to evolving standards or user requirements, and easy modification during their development or even their field use. The system and technology complexity results in serious design and development challenges, such as reduction of the design productivity gap, time-to market and costs for the increasingly complex and sophisticated systems without compromising their quality. There is a general consensus that opportunities created can be effectively

exploited only through use of ***more adequate application-specific system architectures*** and ***more integrated system IP modules***, supported by new ***effective and efficient model-based design methods and electronic design automation (EDA) tools*** for rapid development of high-quality hardware platforms and efficient automatic mapping of applications on the platforms.

This paper focuses on mastering the automatic architecture synthesis and application mapping for heterogeneous customizable multi-processor systems-on-chip (MPSoCs) based on configurable and extensible application-specific instruction-set processors (ASIPs). It presents the results of our analysis of the main problems that have to be solved and challenges to be faced in design of such heterogeneous customizable MPSoCs for modern demanding applications, and briefly discusses the approach proposed in the recently started European research project ASAM (Automatic Architecture Synthesis and Application Mapping) of the ARTEMIS Program.

2 Issues and challenges of heterogeneous customizable MPSoC design for highly demanding applications

In the traditional embedded system development approaches, the major development activities are usually largely disjoint and performed by different teams using different supporting tools. This leads to inefficiencies, errors and costly reiterations in development process. Moreover, an existing and stable computation platform (HW platform, compilers etc.) is required, while for the modern embedded systems the architecture, algorithms, hardware and software have to be application-specific, and must be developed largely in parallel. The efficiency of the required parallel development is however much too low, due to lack of effective automated methods of industrial strength for the most embedded MPSoC design problems and weak interoperability of the architecture, algorithm, HW/SW, and hardware synthesis tools. The inefficiencies identified above result in substantially lower than attainable effectiveness and efficiency of the developed systems, much longer than necessary development time, and much higher development costs.

The **architecture platform targeted in the ASAM project** is the ***customizable for specific applications heterogeneous multi-ASIP platform based on configurable and extensible ASIPs***. This platform provides the flexibility required for engineering of robust, context-aware and adaptive systems for many application domains and enables programmable SoCs with performance close to this of hardwired ASICs, but at substantially lower costs and with much shorter times to market than hardwired ASICs. The ASAM project aims to deliver a design methodology and related tool chain for the development of programmable MPSoCs for highly demanding applications traditionally dominated by hardwired solutions. It operates in the context of actual industrial system development frameworks and tools of its industrial partners, and in relation to actual industrial designs, with the ultimate aim of building industry-strength EDA-tools based on the project results.

The **new MPSoC design technology based on adaptable ASIPs** being the subject of the ASAM project ***is relevant for a very broad range of applications*** (e.g.

consumer electronic, multimedia, entertainment, telecom, medical imaging and signal processing, advanced machinery and instrumentation, automotive, military, cross-domain convergence products, etc.) and ***is applicable to several implementation technologies*** (e.g. SOC or ASIC, structured ASIC, and FPGA). This customizable multi-ASIP MPSoC technology is especially suitable for implementation of complex applications involving different kinds of processing with various kinds of parallelism and being highly demanding regarding physical and economic characteristics.

The research and development of the ASAM project is related to and builds on the platform-based design of heterogeneous multi-processor embedded systems (being researched only in the recent years), as well as, hardware compilation techniques (being researched for at least the last two decades, but still requiring much more research), and software compilation techniques (being researched much longer, but still requiring research, a. o. in relation to application parallelism exploitation). Having as its target MPSoCs based on adaptable ASIPs, it addresses a coherent system-level synthesis and prototyping flow, involving the application-specific system-level architecture synthesis, module-level micro-architecture synthesis, as well as application and technology-specific hardware and software implementation and optimization, all based on the application analysis. In the traditional development approaches, these development activities are usually largely disjoint and performed by different teams using different supporting tools, and this causes substantial inefficiencies. However, the systemic realizations of complex and highly demanding applications, for which the customizable multi-ASIP MPSoC technology is especially suitable, demand the performance and energy usage levels comparable to those of ASICs, while remaining small-size and cost-effective. Satisfaction of these stringent and often conflicting demands requires efficient exploitation of different kinds of parallelism involved in these applications, implementation of critical parts of their information processing in special-purpose hardware of application-specific functional units and efficient trade-off exploitation among various design characteristics. While most existing methods and tools of custom instruction-set construction are devoted to optimization of a single processor, in a customizable multi-ASIP MPSoC its various ASIPs have to be customized in combination, and in a strict relation to the selection of the number of ASIPs, as well as to the scheduling and mapping of the application's required computations on the particular ASIPs, to result in a high-quality MPSoC. Thus, the MPSoC macro-architecture and the micro-architectures of its particular ASIPs are strictly interrelated. There are many trade-offs regarding the granularity of individual processing cells and between the amount of parallelism and resources at each of the two architecture levels (e.g. similar performance can be achieved with fewer processors, each being more parallel and better targeted to particular part of application, as with more processors, each being less parallel and less application-specific). A lot of communication is required during the multi-ASIP MPSoC synthesis between the macro- and micro-architecture synthesis tasks to arrive at a satisfactory MPSoC architecture. The aim here is to find an adequate balance between the number of parallel processors, the complexity of the inter-processor communication, and the intra-processor parallelism and complexity.

Moreover, the custom instruction set construction is very simplistic in most of the current methods. It is usually based on some proxy attributes and optimization

objectives, on a kind of simplified application analysis, performed without actually accounting for the related data-path and control-path implementation, and without accounting for the effects and trade-offs of hardware sharing by various instructions. In result, the proxy formulations of the custom instruction set construction problems and their suggested solutions do not reflect well the actual problems to be solved and their required solutions. Additionally to the instruction-set selection, there is a plethora of other architectural choices on the micro-architectural level, as selection of the number of parallel instructions and issue slots, the number of register files, ports and registers, grouping the issue slots into clusters, interconnects between clusters, etc.

Finally, many modern applications require hardware implementation of algorithms that involve complex interrelationships between the data and computing operations. For applications of this kind, the main design problems are related to an adequate resolution of memory and communication bottlenecks and to decreasing the memory and communication hardware complexity. Moreover, the memory and communication structure design, and micro-architecture design for computing units cannot be performed independently, because they substantially influence each other.

3 Aim and approach of the ASAM project

The main aim of the project is **to improve the MPSoC design efficiency**, while substantially improving the result quality, **through an adequate system and sub-system level design exploration and uniform automatic HW/SW compilation** of application specifications into their highly optimized application-specific heterogeneous multi-ASIP implementations. The uniform design flow will provide efficient exploration of the architecture and application mapping tradeoffs. The compilation process will efficiently select processor types needed, reuse and instantiate available processors, and extend them with instruction sets implemented as parts of new application-specific data-paths. The result of the proposed design exploration and architecture synthesis will integrate the most appropriate ASIP processor types, selected to implement various parallel computations patterns, and application-specific hardware, implementing the most critical computation and data intensive application parts.

This aim will be realized through development of **a unified synthesis and prototyping environment** enabling:

- ***technology-aware multi-objective design space exploration for customizable heterogeneous multi-ASIP SoCs and construction of the application-tailored system architecture*** (i.e. decision on: the number of processors of each kind; kind and shape of communication resources and memory hierarchy; their composition; and scheduling and mapping of the application computation processes on the hardware platform);
- ***architecture instantiation or synthesis of particular application-tailored processors, and communication and memory structures***;
- ***adequate hardware synthesis*** of the designed hardware platform architecture,

- ***software compiler retargeting and (semi-)automatic application mapping on the resulting multi-processor platform***, when accounting for the processor characteristics and for the functional and extra-functional requirements and trade-offs.

This way a consistent highly efficient automatic synthesis flow will be created from the algorithmic specification down to its hardware/software implementation at the circuit/code level. ***The new automated coherent design environment will enable the system and algorithm designers to perform rapid exploration of the high-level design and algorithm solution spaces, automate the final system synthesis***, and in consequence, ***quickly develop high-quality designs***.

With respect to MPSoC macro-architecture synthesis, the project builds on the quality-driven model-based architecture exploration and synthesis approach [1][2] and modelling, emulation, estimation and design exploration concepts [2][4] earlier developed by some of the project partners. It will develop a new architecture methodology and supporting tools that will enable an effective and efficient reuse of a generic architecture platform and platform modeling in the form of an abstract architecture template, generic architecture template instantiation, abstract requirement modeling, application process scheduling and mapping on the generic architecture template instance when observing the constraints objectives and tradeoffs of the requirement model, and final architecture refinement and optimization.

The ASIP micro-architecture synthesis will perform the final processor data-path and control-path construction when re-using the existing application-class specific and generic ASIP IP cores customizable for a specific application. It has to identify parts of the application that require specialized hardware through finding operation patterns to be replaced by new instructions, define sequences of operations that can operate independently on separated hardware clusters and local register files, and construct the corresponding instruction set hardware clusters, register files, memories, and other processor parts, when adequately accounting for hardware reuse and satisfying the application's constraints, objectives and trade-offs. The existing commercial and academic developments in this field do not provide adequate support for this critical part of the designers' work. Therefore, new methods will be developed in the scope of the project to much better reflect the actual problems to be solved and their required solutions in the proxy formulations and solutions of the new method.

As explained in the previous section, there are very strong interrelations between the macro- and micro-architecture synthesis of heterogeneous MPSoCs based on configurable and extendable ASIPs. Therefore, in our architecture synthesis method the macro-architecture and micro-architecture synthesis will represent one coherent complex system architecture synthesis task, and not two separate tasks, as in the state-of-the-art methods. There will be common aims and a strong consistent communication between the two sub-tasks.

Since many modern applications require hardware implementation of algorithms that involve complex interrelationships between the data and computing operations, the project builds on recent results of one of the project partners [5][6] to develop new methods and tools for the application-tailored and technology aware interconnects and memory structures construction.

From the above it should be clear that during the multi-ASIP MPSoC synthesis a lot of collaboration and communication is required between the various models used,

as well as the macro- and micro-architecture synthesis, and various other tasks, to arrive at a satisfactory MPSoC design. The success of the approach proposed heavily depends on the compatibility and coherent collaboration of all the models and tools. Ensuring adequate model and tool interoperability is one of its main challenges. This involves both the vertical interoperability between the different system design levels and the horizontal interoperability among the models and tools dealing with different design aspects at the same level.

4 Conclusion

This paper presented the results of our analysis of the main problems and challenges to be faced in the design of heterogeneous customizable ASIP-based MPSoCs for modern demanding applications, and briefly discussed the approach proposed in the recently started European research project ASAM. Further problem analysis and workout of the approach proposed into actual effective and efficient methods and tools will make it possible to achieve the main aim of the project, i.e. to improve the MPSoC design efficiency for actual industrial designs.

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